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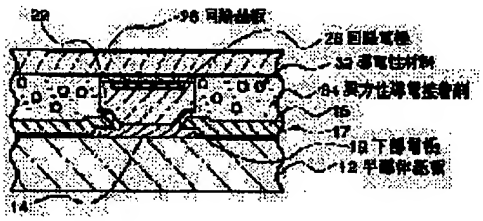
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD AND CONNECTION STRUCTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To avoid floating of the conductive material between a bump electrode and a circuit electrode by a method wherein, within an insulating film having an aperture part in the periphery on an electrode pad, a lower part electrode film pr vided on the electrode pad and a semiconductor device having a bump electrode, the central part of the crest of the bump electrode is made lower than th periphery.



SOLUTION: An inorganic insulating film 17 and an organic insulating film 15 having aperture parts in an electrode pad 14 on the same plane as well as a lower part electrode 19 connecting to the electrode pad 14 and a protruding electrode 22 connecting to the lower part electrode 19 are provided on a semiconductor substrate 12. Furthermore, the plane shape of the bump electrode 22 is made larger than the aperture dimensions of the inorganic insulating film 17 and the organic insulating film as well as the central part of the crest of the bump electrode 22 is composed lower than the periphery. At this time, the periphery of the crest of the protruding electrode 22 is composed higher than the central part. In such a constitution, the floating conductive material 32 between the bump electrode 22 and the circuit electrode 28 on a circuit substrate 26 together with an anisotropical conductive adhesive 34 from connecting surface in the case of connection pressurization can be avoided.

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CLAIMS

[Claim(s)]

[Claim 1] It is the semiconductor device characterized by being the semiconductor device which has the insulator layer which has opening in the periphery section on an electrode pad, the lower electrode layer prepared on an electrode pad, and a salient electrode, and the crowning of a salient electrode having a center section lower than the periphery section.

[Claim 2] It is the semiconductor device characterized by being a semiconductor device according to claim 1, and for an insulator layer consisting of two-layer [of an inorganic film and an organic film], and the center section of the salient electrode, the level difference of the periphery section, and the thickness of an insulator layer being almost the same.

[Claim 3] It is the semiconductor device characterized by being a semiconductor device according to claim 2, and for the configuration of the inorganic insulator layer of the electrode pad periphery section and an organic compound insulator being the same configuration mostly, and the center section of the salient electrode, the level difference of the periphery section, and the thickness of an insulator layer being almost the same.

[Claim 4] It is the semiconductor device which it is a semiconductor device according to claim 2, and an insulator layer consists of two-layer [of an inorganic film and an organic film], arranges the configuration of the electrode pad periphery section of an organic film in the periphery section from an inorganic film, and is characterized by the center section of the salient electrode, the level difference of the periphery section, and the thickness of an organic film being almost the same.

[Claim 5] It is the semiconductor device characterized by being a semiconductor device according to claim 1, and for an insulator layer consisting of an inorganic film and the center section of the salient electrode, the level difference of the periphery section, and the thickness of an inorganic film being almost the same.

[Claim 6] It is the semiconductor device characterized by being a semiconductor device according to claim 1, and for an insulator layer consisting of an organic film and the center section of the salient electrode, the level difference of the periphery section, and the thickness of an organic film being almost the same.

[Claim 7] The manufacture method of a semiconductor device characterized by providing the following. The process which forms a common electrode layer on the whole surface on the semiconductor device which has opening of the insulator layer to which the center section of the salient electrode, the level difference of the periphery section, and the thickness of an insulator layer have the same thickness on an electrode pad. The process which carries out patterning of the photopolymer. The process which hydrophilicity--ization-processes a photopolymer front face. The process which forms a salient electrode in photopolymer opening, the process which removes a photopolymer, and the process which uses a salient electrode as a mask and carries out patterning of the common electrode layer.

[Claim 8] It is the connection structure of the semiconductor device characterized by connecting with the circuit electrode which is the connection structure of a semiconductor device of having the insulator layer which has opening in the periphery section on an electrode pad, the lower electrode layer prepared on an electrode pad, and a salient electrode, and the crowning of a salient electrode has a center section lower than a periphery, and a conductive material is secured in the crevice of a salient electrode, and meets.

[Claim 9] It is the connection structure of the semiconductor device characterized by being the connection structure of the semiconductor device of a claim 8, and the particle size of a conductive material being larger than the level difference size of a salient electrode crowning.

[Claim 10] It is the connection structure of the semiconductor device characterized by being the connection structure of the semiconductor device of a claim 8, and the particle size of a conductive material being almost the same as the level difference size of a salient electrode crowning, or being small.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates a semiconductor device to the connection structure to the circuit board using this salient electrode further about the structure and its manufacture method of the salient electrode which makes electric and mechanical connection to the circuit board.

[0002]

[Description of the Prior Art] it has the cross section of drawing 11 - drawing 15 , and the manufacture method for forming the structure of the salient electrode of the straight wall configuration in a Prior art and this structure is,

and is explained
[0003] [-- salient electrode structure: -- drawing 15] -- it is with drawing 15 first and the salient electrode structure of the conventional technology is explained On the semiconductor substrate 12, an insulator layer 16 is formed so that opening of the electrode pad 14 may be carried out, and a common electrode layer is formed all over the so that it may be shown in drawing 15 . Furthermore, the salient electrode 22 is formed in a straight wall configuration, a common electrode layer is **********ed and the semiconductor device which has the salient electrode 22 is formed.
[0004] Connection with the circuit electrode 28 formed in the circuit board 26 is made with the anisotropy electric conduction adhesives 34 which made the conductive material 32 intermingled in a semiconductor device and insulating adhesives by this salient electrode 22. The conductive material 32 performs electrical installation of the salient electrode 22 and the circuit electrode 28, and mechanical connection between a semiconductor device and the circuit board is made with insulating adhesives.
[0005] by adopting the manufacture method of the salient electrode 22 of the straight wall configuration in this conventional technology, it is able for a cross-section configuration not to have a spread by the longitudinal direction of ****** and a salient electrode in the mushroom configuration where a crowning is bigger than a root, and to form in the flat-surface configuration which a salient electrode crowning can connect with the conductive material 32 For this reason, in the salient electrode 22 of a straight wall configuration, there is an advantage which can carry out [detailed]-izing of the connection pitch.
[0006] [-- manufacture ******: of a salient electrode -- drawing 11 - drawing 15] -- the manufacture method of the straight wall salient electrode in this Prior art is explained using the cross section of drawing 11 - drawing 15 below
[0007] The whole surface on the semiconductor substrate 12, an insulator layer 16 is formed and the insulator layer 16 which has opening so that the electrode pad 14 may be exposed is formed with photo etching technology so that it may be first shown in drawing 11 .
[0008] The common electrode layer 18 is formed in the whole surface by the sputtering method so that it may next be shown in drawing 12 . This common electrode layer 18 forms 0.8 micrometers and chromium by 0.01 micrometers, and forms copper for the semiconductor substrate 12 side to aluminum one by one by the thickness of 0.8 micrometers. As for the common electrode layer 18 with this multilayer structure, a role of an electrode when forming a salient electrode by the galvanizing method both also has the role of a connection layer with the electrode pad 14, and the barrier layer which prevents counter diffusion.
[0009] Then, a photopolymer 20 is formed in the whole surface by the thickness of 17 micrometers by the rotation applying method, and with photo lithography technology, it forms so that it may have opening in the salient electrode 22 formation section.
[0010] The salient electrode 22 of a straight wall configuration is formed by the thickness of 10 micrometers - 15 micrometers by gold plate so that it may next be shown in drawing 13 .
[0011] Then, the salient electrode 22 is used as a mask, the common electrode layer 18 is **********ed by the wet etching method, and the semiconductor device which forms the lower electrode 19 and has a salient electrode is formed so that it may be shown in drawing 14 .
[0012] In order for the common electrode layer 18 to have 0.8 micrometers and chromium formed by 0.01 micrometers and to form copper by the three-tiered structure by the thickness of 0.8 micrometers in the semiconductor substrate 12 side to the aluminum, the reason for adopting wet etching as etching processing of the common electrode layer 18 here must choose compound etching gas for etching gas intricately by the dry etching method, in order to obtain the etch selectivity of an etched layer and other layers.
[0013] The duration for carrying out etching processing still in industrial production starts very long, and it has the fault from which a processor will also become expensive.
[0014] However, by the wet etching method, etching processing can be performed for a large-scale facility to ****** simple by choosing the etching reagent which can take etch selectivity.
[0015] Then, a dicing process performs cutting processing for the semiconductor substrate 12 to the semiconductor chip of a single individual.
[0016] It is made to intervene between the circuit boards 26 which have two or more circuit electrodes 28 which carried out confrontation arrangement of the anisotropy electric conduction adhesives 34 which made the electrical conducting material 32 intermingled in insulating adhesives with the semiconductor substrate 12 which has two or more salient electrodes 22, and pressurization and heating are added between the salient electrode 22 and the circuit electrode 26 so that it may next be shown in drawing 15 .
[0017] The conductive material 32 is secured between the salient electrode 22 and the circuit

electrode 28 by this, and electric and opportunity-connection of the salient electrode 22 and the circuit electrode 28 is made.
[0018]
[Problem(s) to be Solved by the Invention] However, with the structure, the conventional manufacture method, and its conventional connection structure of the salient electrode 22, the anisotropy electric conduction adhesives 34 which made the conductive material 32 intermingled are intervened between the salient electrode 22 and the circuit electrode 28, the conductive material 32 will flow out of between the salient electrode 22 and the circuit electrode 28 at the time of heating pressurization, and the number of the conductive material 32 between the salient electrode 22 and the circuit electrode 28 will decrease extremely at it.
[0019] In order to secure sufficient connection resistance (0.1ohms or less of the first stage) and sufficient high-reliability, the number of the conductive material 32 which intervenes between the salient electrode 22 and the circuit board 28 is the ten or more piece need.
[0020] As for the conductive material 32 made intermingled in epoxy system adhesives, nickel gold is formed in the front face of a plastics bead whose diameter is 5 micrometers. The connection resistance per piece of this conductive material 32 is about 1ohm, and the connection resistance 1000 hours [in the temperature of 85 degrees C / 85% atmosphere of humidity] after a high-humidity/temperature reliability trial can be set to 1ohm or less by setting early connection resistance to 0.1 ohms.
[0021] The reason the connection resistance at this time rises is for the connection area of the conductive material 32 to fall, when adhesive strength declines by degradation of the epoxy system adhesives which are the insulating adhesives between the salient electrode 22 and the circuit board 28 and salient electrode 22 and circuit electrode 26 interval spreads.
[0022] For this reason, in order to secure the ten or more number of the conductive material 32, it is the area of the salient electrode 22 6000 micrometers 2 You have to carry out above. Therefore, in the Prior art, it was very difficult to make detailed pitch connection which moreover has high-reliability with low connection resistance.
[0023] [the purpose of invention] -- it is the flow of a salient electrode and a circuit inter-electrode conductive material which the purpose of this invention solves the above-mentioned technical problem, and generates at the time of connection pressurization -- it is offering the semiconductor device and the manufacture method of preventing **, fully securing the number of a salient electrode and circuit inter-electrode conductive material, raising connection reliability, making connection area small further, and having detailed-izing of a connection pitch, and high-reliability, and its connection structure
[0024]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the means of the following publication is adopted in the semiconductor device, its manufacture method, and its connection structure of this invention.
[0025] The structure of the semiconductor device of this invention is a semiconductor device which has the insulator layer which has opening in the periphery section on an electrode pad, the lower electrode layer prepared on an electrode pad, and a salient electrode, and the crowning of a salient electrode is characterized by a center section being lower than the periphery section.
[0026] With the structure of the semiconductor device of this invention, an insulator layer consists of two-layer [of an inorganic film and an organic film], and is characterized by the center section of the salient electrode, the level difference of the periphery section, and the thickness of an insulator layer being almost the same.
[0027] With the structure of the semiconductor device of this invention, the configuration of the insulator layer of the electrode pad periphery section is the same configuration mostly, and it is characterized by the center section of the salient electrode, the level difference of the periphery section, and the thickness of an insulator layer being the same.
[0028] With the structure of the semiconductor device of this invention, an insulator layer consists of two-layer [of an inorganic film and an organic film], and the configuration of the electrode pad periphery section of an organic film is arranged in the periphery section from an inorganic film, and is characterized by the center section of the salient electrode, the level difference of the periphery section, and the thickness of an organic film being almost the same.
[0029] With the structure of the semiconductor device of this invention, an insulator layer consists of an inorganic film and is characterized by the center section of the salient electrode, the level difference of the periphery section, and the thickness of an inorganic film being almost the same.
[0030] With the structure of the semiconductor device of this invention, an insulator layer consists of an organic film and is characterized by the

center section of the salient electrode, the level difference of the periphery section, and the thickness of an organic film being the same.
[0031] In the manufacture method of the semiconductor device of this invention on an electrode pad The center section of the salient electrode, and the level difference of the periphery section, The process which forms a common electrode layer on the whole surface on the semiconductor device which has opening of an insulator layer in which the thickness of an insulator layer has the same thickness, It is characterized by having the process which carries out patterning of the photopolymer, the process which hydrophilicity--ization-processes a photopolymer front face, the process which forms a salient electrode in photopolymer opening, the process which removes a photopolymer, and the process which uses a salient electrode as a mask and carries out patterning of the common electrode layer.
[0032] It is the semiconductor device which has the insulator layer which has opening in the periphery section on an electrode pad, the lower electrode layer prepared on an electrode pad, and a salient electrode in the connection structure of the semiconductor device of this invention, and the crowning of a salient electrode has a center section lower than a periphery, and it is characterized by a conductive material connecting with the circuit electrode which is secured in the crevice of a salient electrode and meets.
[0033] With the connection structure of the semiconductor device of this invention, particle size of a conductive material is characterized by being larger than the level difference size of a salient electrode crowning.
[0034] With the connection structure of the semiconductor device of this invention, particle size of a conductive material is characterized by being almost the same as the level difference size of a salient electrode crowning, or being small.
[0035] [Operation] The center section of the salient electrode crowning makes the structure, the manufacture method, and connection structure of a semiconductor device by this invention lower than the periphery section. When connection pressurization of the conductive material between a salient electrode and a circuit electrode is carried out by this, it stops flowing out with a flow of anisotropy electric conduction adhesives, and sufficient number can secure a conductive material between a salient electrode and a circuit electrode by it.
[0036] By a still more sufficient number of conductive material being securable, salient electrode area can be made small and it becomes possible to offer highly reliable connection moreover in a detailed pitch.
[0037]
[Embodiments of the Invention] The structure, the manufacture method, and connection structure of a semiconductor device in the best form for carrying out this invention using a drawing below are explained. Drawing 1 · drawing 10 are the cross sections and plans in which are attained to in the structure and the manufacture method of a semiconductor device of this invention, and connection structure is shown. Drawing 5 is used first and the structure and connection structure of a semiconductor device of this invention are explained.
[0038] [-- the structure of the semiconductor device of this invention, and connection structure explanation: -- drawing 5 and drawing 6] -- on the semiconductor substrate 12, the inorganic insulator layer 17 which has opening in the electrode pad 14, and an organic compound insulator 15 are formed in the same flat-surface configuration, and the lower electrode 19 linked to the electrode pad 14 and the salient electrode 22 linked to the lower electrode 19 are formed Furthermore, as the flat-surface configuration of the salient electrode 22 is shown in drawing 6 , in consideration of the degree of etching margin of the lower electrode 19, it forms greatly 5 micrometers · 10 micrometers from the opening size of the inorganic insulator layer 17 and an organic compound insulator 15, and a center section constitutes the crowning of the salient electrode 22 from the periphery section in a low configuration.
[0039] The periphery section of the crowning of the salient electrode 22 at this time is constituted so that it may become higher 2-5 micrometers than a center section. Thus, by making the periphery section of salient electrode 22 crowning higher than a center section, in case the conductive material 32 between the salient electrode 22 and the circuit electrode 28 on the circuit board 26 is connection pressurization, it prevents flowing from a connection side with the anisotropy electric conduction adhesives 34, and a sufficient number for a connection side of conductive material 32 is secured, and the quality of a semiconductor device is improved.
[0040] [-- semiconductor device of this invention manufacture method explanation: -- drawing 1 · drawing 10] -- the manufacture method of the semiconductor device of the structure shown in this drawing 5 next is explained, and it is the plan in which the electrode pad section of the

semiconductor device by this invention is shown, and with a cross section and a plan, drawing 6 , drawing 8 , and drawing 10 are, and are explained

[0041] The inorganic insulator layer 17 and an organic compound insulator 15 are formed in the same configuration so that it may be shown in drawing 1 , and opening of the electrode pad 14 which consists of aluminum on the semiconductor substrate 12 in which the predetermined element was formed may be carried out.

[0042] This inorganic insulator layer 17 forms a silicon nitride in the whole surface by the thickness of 1 micrometer by the plasma-chemistry-vapor growth.

[0043] A silicon dioxide, tantalum oxide, and inorganic films of this inorganic insulator layer 17, such as oxidization aluminum, are also effective in addition to a silicon nitride. Furthermore as the film formation method, it can form also by the sputtering method in addition to a plasma-chemistry-vapor growth.

[0044] Next, for example, a photosensitive polyimide is formed in the whole surface by the thickness of 2 micrometers - 3 micrometers by the rotation applying method as an organic compound insulator 15.

[0045] Then, opening of the electrode pad 14 is carried out according to a photo etching process, and patterning of an organic compound insulator 15 is performed so that it may moreover lap in the periphery section of the electrode pad 14.

[0046] Then, an organic compound insulator 15 is used as a mask, it etches by having carbon tetrafluoride or etching gas of a sulfur hexafluoride, and the inorganic insulator layer 17 being by the dry etching method, and the inorganic insulator layer 17 is formed in the same pattern configuration as an organic compound insulator 15. The flat-surface configuration pattern configuration at this time is shown in the alternate long and short dash line of the drawing 6 plan.

[0047] the reason for forming an organic compound insulator 15 on the inorganic insulator layer 17 is because it is possible to form the level difference of 3 micrometers - 5 micrometers in the periphery section of an electrode pad simple as the stress relaxation effect of the salient electrode 22

[0048] Then, all over an organic-compound-insulator 15 top, by the sputtering method, 0.8 micrometers is carried out for aluminum, film formation of 0.01 micrometers and the 0.8 micrometers of the copper is carried out for chromium one by one so that it may be shown in drawing 2 , and the common electrode layer 18 is formed by the three-tiered structure.

[0049] This common electrode layer 18 does not have the electrode-material mutual diffusion with good electric and mechanical-connections nature with the electrode material formed by the electrode pad 14 and the salient electrode 22, and needs selection of a stable electrode material.

[0050] Two-layer membrane structures, such as titanium-palladium, titanium-gold, titanium-platinum, titanium tungsten alloy-palladium, titanium tungsten alloy-gold, and titanium tungsten alloy-platinum, and the three-tiered structure of aluminum-titanium-copper of the common electrode 18 are also effective.

[0051] Then, a photopolymer is formed by the thickness of 17 micrometers the whole surface on the common electrode layer 18 by the rotation applying method, exposure and a development are performed using a photo mask, patterning of a photopolymer is performed, and a photopolymer 20 is formed so that it may be shown in drawing 3 .

[0052] Next a photopolymer 20 is used as a plating mask, gilding is formed by the thickness of 10 micrometers - 15 micrometers, and the salient electrode 22 is formed. The flat-surface pattern configuration at this time is shown in the dashed line of drawing 6 .

[0053] Then, it is with wet exfoliation liquid and a photopolymer 20 is removed so that it may be shown in drawing 4 . Furthermore, the salient electrode 22 is used as an etching mask, and the copper which is the best layer coat of the common electrode layer 18 is etched by the Meltex copper etching-reagent engine failure lip C (tradename). In addition, this etching processing etches in 30% of over etching time from just etching.

[0054] Next, the mixed liquor of cerium-nitrate ammonium, potassium ferricyanide, and a sodium hydroxide performs etching of the chromium (middle lamella) which is the barrier layer and adhesion layer of the common electrode layer 18, and aluminum (the lowest layer). In addition, this etching processing etches in 30% of over etching time from just etching. Consequently, the lower electrode 19 is formed and the center section of the crowning of the salient electrode 22 forms a semiconductor device low 3 micrometers - 5 micrometers compared with the periphery section. The flat-surface pattern configuration at this time is shown in the dotted line of drawing 6 .

[0055] The difference of the height of a center section and the periphery section of salient electrode 22 crowning is controlled by formation thickness of the inorganic insulator layer 17 and an organic compound insulator 15.

[0056] A dicing process performs the

semiconductor substrate 12 to the next, and it cuts to the semiconductor chip of a single individual.
[0057] Then, heat-hardened type epoxy system adhesives are made to be placed between the front faces of spherical plastics as insulating adhesives between the circuit boards 26 which have two or more circuit electrodes 28 which carried out facing arrangement of the anisotropy electric conduction adhesives 34 with which two-layer plating of the nickel-gold was carried out, and which made the conductive material 32 of the shape of a bead with an outer diameter of 4 micrometers - 6 micrometers intermingled about 40% by the volume ratio with the semiconductor substrate 12 which has two or more salient electrodes 22 so that it may be shown in drawing 5 Then, they are 400 kg/cm2 between the salient electrode 22 and the circuit electrode 26. Heating is added at the temperature of 180 degrees C - 220 degrees C, pressurizing by the pressure.
[0058] An electrical conducting material 32 is secured between the salient electrode 22 and the circuit electrode 28 by this, and mechanical electric connection of the salient electrode 22 and the circuit electrode 28 is made.
[0059] [-- semiconductor device explanation [of another operation form]: -- drawing 7 and drawing 8] -- it has the cross section of drawing 7 , and the plan of drawing 8 in the next, the manufacture method, structure, and connection structure in a form of implementation of the 2nd invention are in it, and it explains to it
[0060] The inorganic insulator layer 17 is formed so that it may be shown in drawing 7 , and opening of the electrode pad 14 which consists of aluminum on the semiconductor substrate 12 in which the predetermined element was formed may be carried out.
[0061] This inorganic insulator layer 17 forms a silicon nitride in the whole surface by the thickness of 2 micrometers - 3 micrometers by the plasma-chemistry-vapor growth.
[0062] Moreover, a silicon dioxide, tantalum oxide, and inorganic films of this inorganic insulator layer, such as oxidization aluminum, are also application in addition to a silicon nitride. Furthermore, the film formation method is also applicable also by the sputtering method in addition to a plasma-chemistry-vapor growth.
[0063] Next, a FOTORISO process and an etching process are performed and the inorganic insulator layer 17 is formed. The flat-surface pattern configuration at this time is shown in the alternate long and short dash line of drawing 8 .
[0064] Then, the whole surface on the inorganic insulator layer 17, by the sputtering method, 0.8 micrometers and chromium are carried out by 0.01 micrometers, film formation of the copper is carried out for aluminum one by one by 0.8-micrometer thickness, and the common electrode layer 18 is formed by the three-tiered structure.
[0065] This common electrode layer 18 does not have the electrode-material mutual diffusion with good electric and mechanical-connections nature with the electrode material formed by the electrode pad 14 and the salient electrode 22, and needs selection of a stable electrode material.
[0066] The common electrode 18 can also apply two-layer membrane structures, such as titanium-palladium, titanium-gold, titanium-platinum, titanium tungsten alloy-palladium, titanium tungsten alloy-gold, and titanium tungsten alloy-platinum, and the three-tiered structure of aluminum-titanium-copper.
[0067] Then, a photopolymer is formed by the thickness of 17 micrometers the whole surface on the common electrode layer 18 by the rotation applying method. Then, exposure and development are performed using a photo mask, patterning of a photopolymer is performed, and a photopolymer 20 is formed.
[0068] Next a photopolymer 20 is used as a plating mask, gilding is formed by the thickness of 10 micrometers - 15 micrometers, and the salient electrode 22 is formed. The flat-surface pattern configuration at this time is shown in the dashed line of drawing 8 .
[0069] Then, it is with wet ablation liquid and a photopolymer 20 is removed, the salient electrode 22 is used as an etching mask, and the copper which is the best layer coat of the common electrode layer 18 is etched using the Meltex copper etching-reagent engine failure lip C (tradename). In addition, this etching processing etches in 30% of over etching time from just etching.
[0070] Next, the mixed liquor of cerium-nitrate ammonium, potassium ferricyanide, and a sodium hydroxide performs etching of the chromium (middle lamella) which is the barrier layer and adhesion layer of the common electrode layer 18, and the aluminum (the lowest layer). In addition, this etching processing etches in 30% of over etching time from just etching. Consequently, compared with the periphery section, with the inorganic insulator layer 17, the lower electrode 19 is formed and it forms [the center section of the crowning of the salient electrode 22 is 2-3 micrometer low semiconductor device, and] it. The flat-surface pattern configuration of the lower

electrode 19 at this time is shown in the dotted line of drawing 8 .

[0071] A dicing process performs the semiconductor substrate 12 to the next, and it cuts to the semiconductor chip of a single individual.

[0072] Then, it forms so that it may be shown in drawing 7 , and it may be made to intervene between the circuit boards 26 which have two or more circuit electrodes 28 which carried out confrontation arrangement of the anisotropy electric conduction adhesives 34 which made the conductive material 32 intermingled with the semiconductor substrate 12 which has two or more salient electrodes 22. Then, they are 400 kg/cm2 between the salient electrode 22 and the circuit electrode 26. Heating is added at the temperature of 180-220 degrees C, pressurizing by the pressure.

[0073] In the gestalt of the 2nd operation, the difference of the height of a center section and the periphery section of salient electrode 22 crowning is controlled by formation thickness of the inorganic insulator layer 17. Thus, forming the top configuration which has the level difference structure of the salient electrode 22 only by inorganic insulator layer 17 monolayer can carry out simple. Furthermore, the common electrode layer 18 on the inorganic insulator layer 17 forms a counter diffusion layer by the interface, is high as compared with an organic compound insulator, and has the advantage whose mechanical strength of the salient electrode 22 improves. [adhesion force's]

[0074] [-- semiconductor device explanation [of still more nearly another operation gestalt]: -- drawing 9 and drawing 10] -- it has the cross section of drawing 9 , and the plan of drawing 10 in the next, the structure, the manufacture method, and connection structure in a gestalt of implementation of the 3rd invention are in it, and it explains to it

[0075] The inorganic insulator layer 17 is formed so that it may be shown in drawing 9 , and opening of the electrode pad 14 which consists of aluminum on the semiconductor substrate 12 in which the predetermined element was formed may be carried out.

[0076] This inorganic insulator layer 17 forms a silicon nitride in the whole surface by the thickness of 1 micrometer by the plasma-chemistry-vapor growth.

[0077] This inorganic insulator layer can also apply a silicon dioxide, tantalum oxide, and inorganic films, such as oxidization aluminum, in addition to a silicon nitride. Furthermore, it can form also by the sputtering method as the coat formation method in addition to a plasma-chemistry-vapor growth.

[0078] Next, a FOTORISO process and an etching process are performed and the inorganic insulator layer 17 is formed. The flat-surface pattern configuration at this time is shown in the alternate long and short dash line of drawing 10 .

[0079] Then, for example, a photosensitive polyimide is formed by the thickness of 2 micrometers - 3 micrometers by the rotation applying method as an organic compound insulator 15 the whole surface on the inorganic insulator layer 17.

[0080] Then, exposure processing and a development are performed and an organic compound insulator 15 is formed. The flat-surface pattern configuration of this organic compound insulator 15 is formed so that it may be shown in the two-dot chain line of drawing 10 and may have opening in the periphery section of the inorganic insulator layer 17. The variation of tolerance of the opening edge of the inorganic insulator layer 17 at this time and the opening edge of an organic compound insulator 15 is formed by 3 micrometers - 5 micrometers.

[0081] Then, the whole surface on the inorganic insulator layer 17, by the sputtering method, 0.8 micrometers and chromium are carried out by 0.01 micrometers, film formation of the copper is carried out for aluminum one by one by 0.8-micrometer thickness, and the common electrode layer 18 is formed by the three-tiered structure.

[0082] This common electrode layer 18 does not have the electrode-material mutual diffusion with good electric and mechanical-connections nature with the electrode material formed by the electrode pad 14 and the salient electrode 22, and needs selection of a stable electrode material.

[0083] The common electrode layer 18 can also apply two-layer structures, such as titanium-palladium, titanium-gold, titanium-platinum, titanium tungsten alloy-palladium, titanium tungsten alloy-gold, and titanium tungsten alloy-platinum, and the three-tiered structure of aluminum-titanium-copper.

[0084] Then, a photopolymer is formed by the thickness of 17 micrometers the whole surface on the common electrode layer 18 by the rotation applying method. Then, exposure and development are performed using a photo mask, patterning of a photopolymer is performed, and a photopolymer 20 is formed.

[0085] Next a photopolymer 20 is used as a plating mask, gilding is formed by the thickness of 10 micrometers - 15 micrometers, and the salient

electrode 22 is formed. The flat-surface pattern configuration at this time is shown in the dashed line of drawing 10 .

[0086] then, wet exfoliation liquid -- having -- it is -- a photopolymer 20 -- removing . Furthermore, after that, the salient electrode 22 is used as an etching mask, and the copper which is the best layer metal of the common electrode layer 18 is **********ed by the Meltex copper etching-reagent engine failure lip C (tradename). In addition, this etching processing etches in 30% of over etching time from just etching.

[0087] Next, etching of the chromium (middle lamella) which is the barrier layer and adhesion layer of the common electrode layer 18, and aluminum (the lowest layer) is carried out by the mixed liquor of cerium-nitrate ammonium, potassium ferricyanide, and a sodium hydroxide. In addition, this etching processing etches in 30% of over etching time from just etching. Consequently, compared with the periphery section, with the inorganic insulator layer 17, the lower electrode 19 is formed and it forms [the center section of the crowning of the salient electrode 22 is a semiconductor device low 2 micrometers - 3 micrometers, and] it. The flat-surface pattern configuration of the lower electrode 19 at this time is shown in the dotted line of drawing 10 .

[0088] A dicing process performs the semiconductor substrate 12 to the next, and it cuts to the semiconductor chip of a single individual.

[0089] Then, it is made to intervene between the circuit boards 26 which have two or more circuit electrodes 28 which carried out confrontation arrangement of the anisotropy electric conduction adhesives 34 which made the conductive material 32 intermingled with the semiconductor substrate 12 which has two or more salient electrodes 22 so that it may be shown in drawing 9 . Then, heating is added at the temperature of 180-220 degrees C, pressurizing by the pressure of 400 kg/cm 2 between the salient electrode 22 and the circuit electrode 26.

[0090] Thus, an organic compound insulator 15 is formed in the outside of the inorganic insulator layer 17 with the form of the 3rd operation. The level difference of a center section and the periphery section of the crowning of the salient electrode 22 is controlled by the organic compound insulator 15. Thus, it is possible to offer a semiconductor device according to the simple process which controls the thickness of an organic compound insulator 17 by this invention.

[0091] In addition, although the square explained the flat-surface pattern configuration of the salient electrode 22 in the above explanation, the salient electrode 22 flat-surface configuration is effective also in a hexagon, an octagon, and a circle configuration in addition to a square. with [with the semiconductor device of such a flat-surface pattern configuration] the structure where the center section of salient electrode 22 crowning is lower than the periphery section, it is the flow of a salient electrode and the circuit inter-electrode conductive material 32 generated at the time of the connection pressurization of the anisotropy electric conduction adhesives 34 -- ** can be prevented and carried out, the number of the conductive material 32 between the salient electrode 22 and the circuit electrode 28 can fully be secured, and connection reliability can be raised

[0092] Thus, the semiconductor device formed by this invention makes connection area small, and it becomes possible to offer a semiconductor device and the manufacture method with detailed-izing of a connection pitch, and high-reliability, and its connection structure.

[0093] Furthermore, without carrying out the process top major change of this invention, the amount of [of salient electrode 22 crowning] center section can form low structure simple compared with a periphery, and a very effective semiconductor device, the manufacture method, and connection structure can be offered on industrial production.

[0094]

[Effect of the Invention] By the above explanation, in the structure, the manufacture method, and its connection structure of a semiconductor device of this invention, the center section of the salient electrode crowning makes it lower than the periphery section so that clearly. When connection pressurization of a salient electrode and the circuit inter-electrode conductive material is carried out by this, it stops flowing out with a flow of anisotropy electric conduction adhesives, and sufficient number can secure a conductive material between a salient electrode and a circuit electrode by it.

[0095] Furthermore, in the semiconductor device of this invention, since sufficient conductive material is securable, salient electrode area can be made small, and moreover, highly reliable connection is offered in a detailed pitch.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the cross section showing the semiconductor device and the manufacture

method in an operation gestalt of this invention.
[Drawing 2] It is the cross section showing the semiconductor device and the manufacture method in an operation gestalt of this invention.
[Drawing 3] It is the cross section showing the semiconductor device and the manufacture method in an operation gestalt of this invention.
[Drawing 4] It is the cross section showing the semiconductor device and the manufacture method in an operation gestalt of this invention.
[Drawing 5] It is the cross section showing the semiconductor device in an operation gestalt, and the manufacture method and its connection structure of this invention.
[Drawing 6] It is the plan showing the semiconductor device and the manufacture method in an operation gestalt of this invention.
[Drawing 7] It is the cross section showing the 2nd semiconductor device in an operation gestalt and its connection structure of this invention.
[Drawing 8] It is the plan showing the 2nd semiconductor device and manufacture method in an operation gestalt of this invention.
[Drawing 9] It is the cross section showing the 3rd semiconductor device in an operation gestalt and its connection structure of this invention.
[Drawing 10] It is the plan showing the 3rd semiconductor device and manufacture method in an operation gestalt of this invention.
[Drawing 11] It is the cross section showing the semiconductor device and the manufacture method in a Prior art.
[Drawing 12] It is the cross section showing the semiconductor device and the manufacture method in a Prior art.
[Drawing 13] It is the cross section showing the semiconductor device and the manufacture method in a Prior art.
[Drawing 14] It is the cross section showing the semiconductor device and the manufacture method in a Prior art.
[Drawing 15] It is the cross section showing the semiconductor device in a Prior art, its manufacture method, and its connection structure.
[Description of Notations]
12 Semiconductor Substrate
14 Electrode Pad
15 Organic Compound Insulator
16 Insulator Layer
17 Inorganic Insulator Layer
18 Common Electrode Layer
19 Lower Electrode
20 Photopolymer
22 Salient Electrode
26 Circuit Board
28 Circuit Electrode
32 Conductive Material
34 Anisotropy Electric Conduction Adhesives

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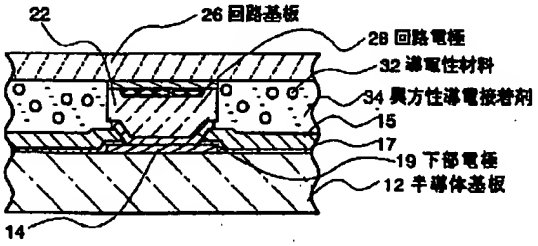
(54)【発明の名称】　半導体装置とその製造方法およびその接続構造

(57)【要約】

【課題】　突起電極と回路電極の間の導電材料が接続時の加熱、加圧の時に流れだしを防止し、充分な接続抵抗値と信頼性を確保する。

【解決手段】　突起電極２２頂部の中央部が周縁部よりも低くし、突起電極２２と回路電極間の導電性材料３２が接続加圧されたときに、異方性導電接着剤３４の流動とともに流れ出すのを抑え、突起電極２２と回路電極２６との間の導電性材料を充分な数が確保できる半導体装置とその製造方法およびその接続構造。



1

【特許請求の範囲】

【請求項１】　電極パッド上の周縁部に開口部を有する絶縁膜と、電極パッド上に設ける下部電極膜と、突起電極とを有する半導体装置であって、

突起電極の頂部は中央部が周縁部より低いことを特徴とする半導体装置。

【請求項２】　請求項１記載の半導体装置であって、

絶縁膜は無機膜と有機膜との２層からなり、

突起電極の中央部と周縁部の段差と絶縁膜の膜厚とがほぼ同じであることを特徴とする半導体装置。

【請求項３】　請求項２記載の半導体装置であって、

電極パッド周縁部の無機絶縁膜と有機絶縁膜との形状はほぼ同一形状であり、

突起電極の中央部と周縁部の段差と絶縁膜の膜厚とがほぼ同じであることを特徴とする半導体装置。

【請求項４】　請求項２記載の半導体装置であって、

絶縁膜は無機膜と有機膜との２層からなり、

有機膜の電極パッド周縁部の形状は無機膜より外周部に配置し、

突起電極の中央部と周縁部の段差と有機膜の膜厚とがほぼ同じであることを特徴とする半導体装置。

【請求項５】　請求項１記載の半導体装置であって、

絶縁膜は無機膜からなり、

突起電極の中央部と周縁部の段差と無機膜の膜厚とがほぼ同じであることを特徴とする半導体装置。

【請求項６】　請求項１記載の半導体装置であって、

絶縁膜は有機膜からなり、

突起電極の中央部と周縁部の段差と有機膜の膜厚とがほぼ同じであることを特徴とする半導体装置。

【請求項７】　電極パッド上に突起電極の中央部と周縁部の段差と絶縁膜の膜厚とが同じ膜厚をもつ絶縁膜の開口を有する半導体装置上に共通電極膜を全面に形成する工程と、

感光性樹脂をパターンニングする工程と、

感光性樹脂表面を親水化処理する工程と、

感光性樹脂開口部に突起電極を形成する工程と、

感光性樹脂を除去する工程と、

共通電極膜を突起電極をマスクにしてパターンニングする工程とを有することを特徴とする半導体装置の製造方法。

【請求項８】　電極パッド上の周縁部に開口部を有する絶縁膜と電極パッド上に設ける下部電極膜と突起電極とを有する半導体装置の接続構造であって、

突起電極の頂部は中央部が周辺部より低く、導電性材料が突起電極の凹部に確保され対面する回路電極と接続することを特徴とする半導体装置の接続構造。

【請求項９】　請求項８の半導体装置の接続構造であって、

導電性材料の粒径は、突起電極頂部の段差寸法より大きいことを特徴とする半導体装置の接続構造。

2

【請求項１０】　請求項８の半導体装置の接続構造であって、

導電性材料の粒径は、突起電極頂部の段差寸法とほぼ同じか小さいことを特徴とする半導体装置の接続構造。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置を回路基板に電気的および機械的な接続を行う突起電極の構造およびその製造方法に関し、さらにこの突起電極を用いた回路基板への接続構造に関する。

【０００２】

【従来の技術】従来の技術におけるストレートウォール形状の突起電極の構造と、この構造を形成するための製造方法を、図１１～図１５の断面図をもちいて説明する。

【０００３】〔突起電極構造：図1､5〕はじめに図１５をもちいて従来技術の突起電極構造を説明する。図１５にしめすように、半導体基板１２上に電極パッド１４を開口するように絶縁膜１６を形成し、その全面に共通電極膜を形成する。さらに、突起電極２２をストレートウォール形状に形成し、共通電極膜をエッチングして、突起電極２２を有する半導体装置を形成する。

【０００４】この突起電極２２により半導体装置と、絶縁性接着剤に導電性材料３２を混在させた異方性導電接着剤３４により、回路基板２６に形成した回路電極２８との接続を行う。突起電極２２と回路電極２８との電気的接続は導電性材料３２によって行い、半導体装置と回路基板との機械的な接続は絶縁性接着剤によって行う。

【０００５】この従来技術におけるストレートウォール形状の突起電極２２の製造方法を採用することにより、断面形状が根元より頂部が大きなマッシュルーム形状にら比べ、突起電極の横方向への広がりがなく、突起電極頂部が導電性材料３２で接続可能な平面形状に形成することが可能である。このためストレートウォール形状の突起電極２２では、接続ピッチを微細化できる利点がある。

【０００６】〔突起電極の製造方法造：図１１～図１５〕つぎにこの従来の技術におけるストレートウォール突起電極の製造方法を、図１１～図１５の断面図を用いて説明する。

【０００７】はじめに図１１にしめすように、半導体基板１２上の全面に、絶縁膜１６を形成し、フォトエッチング技術により、電極パッド１４を露出するように開口部を有する絶縁膜１６を形成する。

【０００８】つぎに図１２にしめすように、共通電極膜１８を全面にスパッタリング法により形成する。この共通電極膜１８は、半導体基板１２側からアルミニュウムを０．８μm、クロムを０．０１μm、銅を０．８μmの厚さで順次形成する。この多層構造をもつ共通電極膜１８は、電極パッド１４との接続層と相互拡散を防ぐバ

リヤ層の役割をもつとともに、突起電極をめっき法にて形成するときの電極としての役割ももつ。

【０００９】その後、感光性樹脂２０を回転塗布法により１７μｍの厚さで全面に形成し、フォトリソグラフィー技術により、突起電極２２形成部に開口を有するように形成する。

【００１０】つぎに図１３にしめすように、金メッキによりストレートウォール形状の突起電極２２を１０μｍ～１５μｍの厚さで形成する。

【００１１】その後、図１４にしめすように、突起電極２２をマスクにして共通電極膜１８を湿式エッチング法によりエッチングし、下部電極１９を形成し突起電極を有する半導体装置を形成する。

【００１２】ここで共通電極膜１８のエッチング処理として、湿式エッチングを採用する理由は、共通電極膜１８は、半導体基板１２側からアルミニュウムを０．８μｍ、クロムを０．０１μｍ、銅を０．８μｍの厚さで３層構造で形成されるため乾式エッチング法では、被エッチング層と他層とのエッチング選択比を得るためにエッチングガスを複合エッチングガスを複雑に選択しなければならない。

【００１３】さらに工業生産的にエッチング加工するための所要時間が非常に長くかかり、処理装置も高価なものとなってしまう欠点を有する。

【００１４】しかしながら、湿式エッチング法ではエッチング選択比のとれるエッチング液を選択することで、大がかりな設備を要さずに簡便にエッチング処理を行うことができる。

【００１５】その後、ダイシング工程により半導体基板１２を単個の半導体チップに切断処理を行なう。

【００１６】つぎに図１５にしめすように、絶縁性接着剤に導電材料３２を混在させた異方性導電接着剤３４を、複数の突起電極２２を有する半導体基板１２と対面配置した複数の回路電極２８を有する回路基板２６との間に介在させ、突起電極２２と回路電極２６間に加圧と加熱を加える。

【００１７】このことにより、突起電極２２と回路電極２８との間に導電性材料３２が確保され、突起電極２２と回路電極２８の電気的・機会的な接続を行う。

【００１８】

【発明が解決しようとする課題】しかしながら従来の突起電極２２の構造と製造方法およびその接続構造では、突起電極２２と回路電極２８の間に導電性材料３２を混在させた異方性導電接着剤３４を介在し、加熱加圧のときに、導電性材料３２が突起電極２２と回路電極２８間から流れだし、突起電極２２と回路電極２８の間の導電性材料３２の数が極端に減少してしまう。

【００１９】充分な接続抵抗値（初期０．１Ω以下）と高信頼性を確保するためには、突起電極２２と回路基板２８との間に介在する導電性材料３２の数が１０個以上必要である。

【００２０】エポキシ系接着剤中に混在させた導電性材料３２は、直径が５μｍのプラスチックビーズの表面にニッケル一金が形成されている。この導電性材料３２の１個当たりの接続抵抗値は約１Ωであり、初期の接続抵抗値を０．１Ωにすることで、温度８５℃／湿度８５％雰囲気における高温高湿信頼性試験１０００時間後の接続抵抗値を１Ω以下にすることができる。

【００２１】このときの接続抵抗値が上昇する理由は、突起電極２２と回路基板２８との間の絶縁性接着剤であるエポキシ系接着剤の劣化により接着力が低下し、突起電極２２と回路電極２６間隔が広がることによって、導電性材料３２の接続面積が低下するためである。

【００２２】このため導電性材料３２の数を１０個以上確保するためには、突起電極２２の面積を６０００μｍ^{2}以上にしなければならない。そのため従来の技術では、低接続抵抗値でしかも高信頼性のある微細ピッチ接続を行うことが非常に困難であった。

【００２３】〔発明の目的〕本発明の目的は、上記課題を解決し、接続加圧時に発生する突起電極と回路電極間の導電性材料の流れだしを防止し突起電極と回路電極間の導電性材料の数を充分に確保し、接続信頼性を向上させさらに、接続面積を小さくして、接続ピッチの微細化と高信頼性のある半導体装置および製造方法とその接続構造を提供することである。

【００２４】

【課題を解決するための手段】上記目的を達成するために本発明の半導体装置およびその製造方法およびその接続構造においては、下記記載の手段を採用する。

【００２５】本発明の半導体装置の構造は、電極パッド上の周縁部に開口部を有する絶縁膜と、電極パッド上に設ける下部電極膜と、突起電極とを有する半導体装置であって、突起電極の頂部は中央部が周縁部より低いことを特徴とする。

【００２６】本発明の半導体装置の構造では、絶縁膜は無機膜と有機膜との２層からなり突起電極の中央部と周縁部の段差と、絶縁膜の膜厚とがほぼ同じであることを特徴とする。

【００２７】本発明の半導体装置の構造では、電極パッド周縁部の絶縁膜の形状はほぼ同一形状であり、突起電極の中央部と周縁部の段差と、絶縁膜の膜厚とが同じであることを特徴とする。

【００２８】本発明の半導体装置の構造では、絶縁膜は無機膜と有機膜との２層からなり有機膜の電極パッド周縁部の形状は、無機膜より外周部に配置し、突起電極の中央部と周縁部の段差と、有機膜の膜厚とがほぼ同じであることを特徴とする。

【００２９】本発明の半導体装置の構造では、絶縁膜は無機膜からなり、突起電極の中央部と周縁部の段差と、無機膜の膜厚とがほぼ同じであることを特徴とする。

5

【００３０】本発明の半導体装置の構造では、絶縁膜は有機膜からなり、突起電極の中央部と周縁部の段差と、有機膜の膜厚とが同じであることを特徴とする。

【００３１】本発明の半導体装置の製造方法においては、電極パッド上に突起電極の中央部と周縁部の段差と、絶縁膜の膜厚とが同じ膜厚をもつ絶縁膜の開口を有する半導体装置上に共通電極膜を全面に形成する工程と、感光性樹脂をパターンニングする工程と、感光性樹脂表面を親水化処理する工程と、感光性樹脂開口部に突起電極を形成する工程と、感光性樹脂を除去する工程と、共通電極膜を突起電極をマスクにしてパターンニングする工程を有することを特徴とする。

【００３２】本発明の半導体装置の接続構造においては、電極パッド上の周縁部に開口部を有する絶縁膜と、電極パッド上に設ける下部電極膜と、突起電極とを有する半導体装置であって、突起電極の頂部は中央部が周辺部より低く、導電性材料が突起電極の凹部に確保され対面する回路電極と接続することを特徴とする。

【００３３】本発明の半導体装置の接続構造では、導電性材料の粒径は、突起電極頂部の段差寸法より大きいことを特徴とする。

【００３４】本発明の半導体装置の接続構造では、導電性材料の粒径は、突起電極頂部の段差寸法とほぼ同じか小さいことを特徴とする。

【００３５】〔作用〕本発明による半導体装置の構造と製造方法および接続構造は、突起電極頂部の中央部が周縁部よりも低くしている。このことによって、突起電極と回路電極との間の導電性材料が接続加圧されたときに、異方性導電接着剤の流動とともに流れ出すのを抑え、突起電極と回路電極との間の導電性材料を充分な数が確保できる。

【００３６】さらに充分な数の導電性材料を確保することができることによって、突起電極面積を小さくすることができ、微細ピッチでしかも高信頼性の接続を提供することが可能となる。

【００３７】

【発明の実施の形態】以下図面を用いて本発明を実施するための最良の形態における半導体装置の構造および製造方法および接続構造を説明する。図１～図１０は本発明の半導体装置の構造と製造方法をおよび接続構造をしめす断面図および平面図である。まずはじめに図５を用いて本発明の半導体装置の構造および接続構造を説明する。

【００３８】〔本発明の半導体装置の構造および接続構造説明：図５および図６〕半導体基板１２上に電極パッド１４に開口部を有する無機絶縁膜１７と、有機絶縁膜１５を同一平面形状で設け、電極パッド１４と接続する下部電極１９と、下部電極１９と接続する突起電極２２とを設ける。さらに、突起電極２２の平面形状は、図６に示すように下部電極１９のエッチング余裕度を考慮し

6

無機絶縁膜１７および有機絶縁膜１５の開口寸法より５μｍ～１０μｍ大きく形成して、突起電極２２の頂部は中央部が周縁部より低い形状で構成する。

【００３９】このときの突起電極２２の頂部の周縁部は中央部より２～５μｍ高くなるように構成する。このように突起電極２２頂部の周縁部を中央部より高くすることによって、突起電極２２と、回路基板２６上の回路電極２８との間の導電性材料３２が接続加圧の際に異方性導電接着剤３４とともに接続面からの流動するのを防止し、接続面に充分な数の導電性材料３２が確保され、半導体装置の品質を向上する。

【００４０】〔本発明の半導体装置の製造方法説明：図１～図１０〕つぎにこの図５にしめす構造の半導体装置の製造方法を説明する、また図６、図８および図１０は本発明による半導体装置の電極パッド部をしめす平面図であり断面図と平面図をもちいて説明する。

【００４１】図１にしめすように、所定の素子を形成した半導体基板１２上のアルミニウムからなる電極パッド１４を開口するように無機絶縁膜１７と有機絶縁膜１５とを同一形状で形成する。

【００４２】この無機絶縁膜１７は、窒化珪素をプラズマ化学的気相成長法により、全面に１μｍの厚さで形成する。

【００４３】この無機絶縁膜１７は、窒化珪素以外に、二酸化珪素や、酸化タンタルや、酸化アルミニュウムなどの無機膜でも有効である。さらに膜形成方法としては、プラズマ化学的気相成長法以外に、スパッタリング法でも形成可能である。

【００４４】つぎに、有機絶縁膜１５としてたとえば感光性ポリイミドを回転塗布法によって、２μｍ～３μｍの厚さで全面に形成する。

【００４５】その後、フォトエッチング工程により電極パッド１４を開口させ、しかも電極パッド１４の周縁部で重なるように有機絶縁膜１５のパターンニングを行う。

【００４６】その後、有機絶縁膜１５をマスクにして無機絶縁膜１７を乾式エッチング法により、四フッ化炭素あるいは六フッ化イオウのエッチングガスをもちいて、エッチングを行い有機絶縁膜１５と同一パターン形状で無機絶縁膜１７を形成する。このときの平面形状パターン形状を、図６平面図の一点鎖線にしめす。

【００４７】無機絶縁膜１７上に有機絶縁膜１５を形成する理由は、突起電極２２の応力緩和効果と、電極パッドの周縁部に３μｍ～５μｍの段差を簡便に形成することが可能であるためである。

【００４８】その後、図２にしめすように有機絶縁膜１５上全面にスパッタリング法によりアルミニウムを０．８μｍ、クロムを０．０１μｍ、銅を０．８μｍ順次膜形成し、共通電極膜１８を３層構造で形成する。

【００４９】この共通電極膜１８は電極パッド１４およ

び突起電極２２で形成される電極材料との電気的、機械的接続性が良好で電極材料相互の拡散が無く安定な電極材料の選定が必要である。

【００５０】共通電極１８はチタンーパラジウムや、チタンー金や、チタンー白金や、チタン・タングステン合金ーパラジウムや、チタン・タングステン合金ー金や、チタン・タングステン合金ー白金などの２層膜構造や、アルミニウムーチタンー銅の３層構造でも有効である。

【００５１】その後、図３にしめすように、感光性樹脂を回転塗布法により共通電極膜１８上の全面に１７μｍの厚さで形成し、フォトマスクを用いて露光、現像処理を行い、感光性樹脂のパターンニングを行い感光性樹脂２０を形成する。

【００５２】つぎに感光性樹脂２０をメッキマスクにして、金めっきを１０μｍ～１５μｍの厚さで形成し突起電極２２を形成する。このときの平面パターン形状を図６の破線にしめす。

【００５３】その後、図４にしめすように、湿式剥離液をもちいて感光性樹脂２０の除去を行う。さらに、突起電極２２をエッチングマスクにして、共通電極膜１８の最上層被膜である銅を、メルテックス製の銅エッチング液エンストリップＣ（商品名）によりエッチングを行う。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。

【００５４】つぎに硝酸セリウムアンモニウムとフェリシアン化カリウムと水酸化ナトリウムとの混合液により、共通電極膜１８のバリヤ層および密着層であるクロム（中層）、およびアルミニュウム（最下層）のエッチングを行う。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。この結果、下部電極１９を形成して突起電極２２の頂部の中央部が周縁部に比べて３μｍ～５μｍ低い半導体装置を形成する。このときの平面パターン形状を図６の点線にしめす。

【００５５】突起電極２２頂部の中央部と周縁部の高さの差は、無機絶縁膜１７と有機絶縁膜１５の形成膜厚によって制御する。

【００５６】つぎに、ダイシング工程により半導体基板１２を単個の半導体チップに切断を行う。

【００５７】その後、図５にしめすように、絶縁性接着剤としてたとえば熱硬化型エポキシ系接着剤に、球状プラスチックの表面にニッケルー金の２層メッキされた、外径４μｍ～６μｍのビーズ状の導電性材料３２を、体積比で約４０％混在させた異方性導電接着剤３４を複数の突起電極２２を有する半導体基板１２と対面配置した複数の回路電極２８を有する回路基板２６との間に介在させる。その後、突起電極２２と回路電極２６間に４００Ｋｇ／ｃｍ^{2}の圧力で加圧しながら、１８０℃～２２０℃の温度で加熱を加える。

【００５８】このことにより、突起電極２２と回路電極２８の間に導電材料３２が確保されて、突起電極２２と回路電極２８の機械的電気的な接続を行う。

【００５９】〔別の実施形態の半導体装置説明：図７および図８〕つぎに、第２の発明の実施の形態における製造方法と構造および接続構造を、図７の断面図と図８の平面図をもちいて説明する。

【００６０】図７にしめすように、所定の素子を形成した半導体基板１２上のアルミニウムからなる電極パッド１４を開口するように無機絶縁膜１７を形成する。

【００６１】この無機絶縁膜１７は、窒化珪素をプラズマ化学的気相成長法によって、全面に２μｍ～３μｍの厚さで形成する。

【００６２】またこの無機絶縁膜は、窒化珪素以外に二酸化珪素や、酸化タンタルや、酸化アルミニュウムなどの無機膜でも適用である。さらに、膜形成方法もプラズマ化学的気相成長法以外に、スパッタリング法でも適用可能である。

【００６３】つぎに、フォトリソ工程とエッチング工程を行い無機絶縁膜１７を形成する。このときの平面パターン形状は、図８の一点鎖線にしめす。

【００６４】その後、無機絶縁膜１７上の全面にスパッタリング法によって、アルミニウムを０．８μｍ、クロムを０．０１μｍ、銅を０．８μｍの膜厚で順次膜形成し、共通電極膜１８を３層構造で形成する。

【００６５】この共通電極膜１８は、電極パッド１４および突起電極２２で形成される電極材料との電気的、機械的接続性が良好で、電極材料相互の拡散がなく安定な電極材料の選定が必要である。

【００６６】共通電極１８はチタンーパラジウムや、チタンー金や、チタンー白金や、チタン・タングステン合金ーパラジウムや、チタン・タングステン合金ー金や、チタン・タングステン合金ー白金などの２層膜構造や、アルミニウムーチタンー銅の３層構造でも適用可能である。

【００６７】その後、感光性樹脂を回転塗布法により、共通電極膜１８上の全面に１７μｍの厚さで形成する。その後、フォトマスクを用いて露光、現像を行い感光性樹脂のパターンニングを行い感光性樹脂２０を形成する。

【００６８】つぎに感光性樹脂２０をメッキマスクにして、金めっきを１０μｍ～１５μｍの厚さで形成し突起電極２２を形成する。このときの平面パターン形状を図８の破線にしめす。

【００６９】その後、湿式剥離液をもちいて感光性樹脂２０の除去を行い、突起電極２２をエッチングマスクにして共通電極膜１８の最上層被膜である銅を、メルテックス製の銅エッチング液エンストリップＣ（商品名）を使用してエッチングを行う。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。

9

【００７０】つぎに硝酸セリウムアンモニウムとフェリシアン化カリウムと水酸化ナトリウムとの混合液により、共通電極膜１８のバリヤ層および密着層であるクロム（中層）、およびアルミニュウム（最下層）のエッチングを行う。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。この結果、下部電極１９を形成して、突起電極２２の頂部の中央部が周縁部に比べて２～３μｍ低い半導体装置を無機絶縁膜１７をもちいて形成する。このときの下部電極１９の平面パターン形状を図８の点線にしめす。

【００７１】つぎに、ダイシング工程により半導体基板１２を単個の半導体チップに切断を行う。

【００７２】その後、図７にしめすように、導電性材料３２を混在させた異方性導電接着剤３４を、複数の突起電極２２を有する半導体基板１２と対面配置した複数の回路電極２８を有する回路基板２６との間に介在させるように形成する。その後、突起電極２２と回路電極２６間に４００Ｋｇ／ｃｍ^2 の圧力で加圧しながら１８０～２２０℃の温度で加熱を加える。

【００７３】第２の実施の形態においては突起電極２２頂部の中央部と周縁部との高さの差は無機絶縁膜１７の形成膜厚によって制御する。このように無機絶縁膜１７単層のみで突起電極２２の段差構造をもつ頂部形状を形成することが簡便に行うことができる。さらに無機絶縁膜１７上の共通電極膜１８は、その界面で相互拡散層を形成して、付着力は有機絶縁膜に比較して高く、突起電極２２の機械的強度が向上する利点がある。

【００７４】〔さらに別の実施形態の半導体装置説明：図９および図１０〕つぎに、第３の発明の実施の形態における構造と製造方法および接続構造を、図９の断面図と図１０の平面図をもちいて説明する。

【００７５】図９にしめすように、所定の素子を形成した半導体基板１２上のアルミニウムからなる電極パッド１４を開口するように無機絶縁膜１７を形成する。

【００７６】この無機絶縁膜１７は、窒化珪素をプラズマ化学的気相成長法によって、全面に１μｍの厚さで形成する。

【００７７】この無機絶縁膜は窒化珪素以外に、二酸化珪素や、酸化タンタルや、酸化アルミニュウムなどの無機膜も適用できる。さらに被膜形成方法として、プラズマ化学的気相成長法以外に、スパッタリング法でも形成可能である。

【００７８】つぎに、フォトリソ工程とエッチング工程を行い無機絶縁膜１７を形成する。このときの平面パターン形状は、図１０の一点鎖線にしめす。

【００７９】その後、無機絶縁膜１７上の全面に、有機絶縁膜１５としてたとえば感光性ポリイミドを回転塗布法により２μｍ～３μｍの厚さで形成する。

【００８０】その後、露光処理と現像処理を行い、有機絶縁膜１５を形成する。この有機絶縁膜１５の平面パターン形状は、図１０の二点鎖線にしめすように無機絶縁膜１７の外周部に開口をもつように形成する。このときの無機絶縁膜１７の開口端と有機絶縁膜１５の開口端との寸法差は、３μｍ～５μｍで形成する。

【００８１】その後、無機絶縁膜１７上の全面にスパッタリング法により、アルミニウムを０．８μｍ、クロムを０．０１μｍ、銅を０．８μｍの膜厚で順次膜形成し、共通電極膜１８を３層構造で形成する。

【００８２】この共通電極膜１８は、電極パッド１４および突起電極２２で形成される電極材料との電気的、機械的接続性が良好で、電極材料相互の拡散がなく安定な電極材料の選定が必要である。

【００８３】共通電極膜１８は、チタン－パラジウムや、チタン－金や、チタン－白金や、チタン・タングステン合金－パラジウムや、チタン・タングステン合金－金や、チタン・タングステン合金－白金などの２層構造や、アルミニウム－チタン－銅の３層構造も適用できる。

【００８４】その後、感光性樹脂を回転塗布法により共通電極膜１８上の全面に１７μｍの厚さで形成する。その後、フォトマスクを用いて露光、現像を行い感光性樹脂のパターンニングを行い感光性樹脂２０を形成する。

【００８５】つぎに感光性樹脂２０をメッキマスクにして、金めっきを１０μｍ～１５μｍの厚さで形成し突起電極２２を形成する。このときの平面パターン形状を図１０の破線にしめす。

【００８６】その後、湿式剥離液をもちいて感光性樹脂２０の除去する。さらにその後、突起電極２２をエッチングマスクにして共通電極膜１８の最上層メタルである銅をメルテックス製の銅エッチング液エンストリップＣ（商品名）によりエッチングする。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。

【００８７】つぎに硝酸セリウムアンモニウムとフェリシアン化カリウムと水酸化ナトリウムとの混合液によって共通電極膜１８のバリヤ層および密着層であるクロム（中層）、およびアルミニュウム（最下層）のエッチングをする。なおこのエッチング処理は、ジャストエッチングから３０％のオバーエッチング時間でエッチングを行う。この結果、下部電極１９を形成して突起電極２２の頂部の中央部が周縁部に比べて２μｍ～３μｍ低い半導体装置を無機絶縁膜１７をもちいて形成する。このときの下部電極１９の平面パターン形状を図１０の点線にしめす。

【００８８】つぎに、ダイシング工程により半導体基板１２を単個の半導体チップに切断を行う。

【００８９】その後、図９にしめすように、導電性材料３２を混在させた異方性導電接着剤３４を複数の突起電極２２を有する半導体基板１２と対面配置した複数の回

路電極２８を有する回路基板２６との間に介在させる。その後、突起電極２２と回路電極２６間に４００Ｋｇ／ｃｍ^{2}の圧力で加圧しながら１８０～２２０℃の温度で加熱を加える。

【００９０】このように第３の実施の形態では、無機絶縁膜１７の外側に有機絶縁膜１５を形成する。突起電極２２の頂部の中央部と周縁部の段差は有機絶縁膜１５で制御する。このように本発明では、有機絶縁膜１７の膜厚を制御する簡便な工程により、半導体装置を提供することが可能である。

【００９１】なお以上の説明では、突起電極２２の平面パターン形状は四角形で説明したが四角形以外に突起電極２２平面形状は、六角形や、八角形や、円形状でも有効である。このような平面パターン形状の半導体装置でも、突起電極２２頂部の中央部が周縁部より低い構造にすることによって、異方性導電接着剤３４の接続加圧時に発生する突起電極と回路電極間の導電性材料３２の流れだしを防止、し突起電極２２と回路電極２８間の導電性材料３２の数を充分に確保し、接続信頼性を向上させることができる。

【００９２】このようにして本発明により形成した半導体装置は接続面積を小さくして、接続ピッチの微細化と高信頼性のある半導体装置および製造方法とその接続構造を提供することが可能となる。

【００９３】さらに本発明は工程上大きな変更することなく突起電極２２頂部の中央部分が周辺部に比べて低い構造を簡便に形成することができ、工業生産上非常に有効な半導体装置と製造方法および接続構造を提供できる。

【００９４】

【発明の効果】以上の説明で明らかなように、本発明の半導体装置の構造と製造方法およびその接続構造においては突起電極頂部の中央部が周縁部よりも低くする。このことによって、突起電極と回路電極間の導電性材料が接続加圧されたときに、異方性導電接着剤の流動とともに流れ出すのを抑え、突起電極と回路電極との間の導電性材料を充分な数が確保できる。

【００９５】さらに本発明の半導体装置においては、充分な導電性材料を確保することができるため突起電極面積を小さくすることができ、微細ピッチでしかも高信頼性の接続を提供する。

【図面の簡単な説明】

【図１】本発明の実施形態における半導体装置および製造方法を示す断面図である。

【図２】本発明の実施形態における半導体装置および製造方法を示す断面図である。

【図３】本発明の実施形態における半導体装置および製造方法を示す断面図である。

【図４】本発明の実施形態における半導体装置および製造方法を示す断面図である。

【図５】本発明の実施形態における半導体装置と、製造方法およびその接続構造を示す断面図である。

【図６】本発明の実施形態における半導体装置および製造方法を示す平面図である。

【図７】本発明の第２の実施形態における半導体装置とその接続構造を示す断面図である。

【図８】本発明の第２の実施形態における半導体装置および製造方法を示す平面図である。

【図９】本発明の第３の実施形態における半導体装置とその接続構造を示す断面図である。

【図１０】本発明の第３の実施形態における半導体装置および製造方法を示す平面図である。

【図１１】従来の技術における半導体装置および製造方法を示す断面図である。

【図１２】従来の技術における半導体装置および製造方法を示す断面図である。

【図１３】従来の技術における半導体装置および製造方法を示す断面図である。

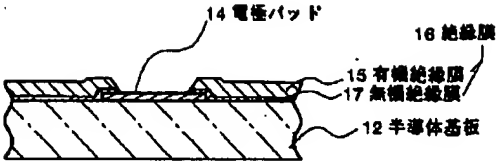
【図１４】従来の技術における半導体装置および製造方法を示す断面図である。

【図１５】従来の技術における半導体装置とその製造方法およびその接続構造を示す断面図である。

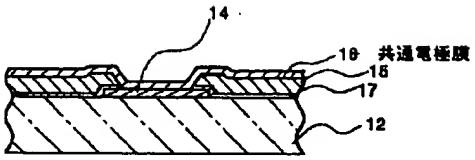
【符号の説明】

１２　半導体基板
１４　電極パッド
１５　有機絶縁膜
１６　絶縁膜
１７　無機絶縁膜
１８　共通電極膜
１９　下部電極
２０　感光性樹脂
２２　突起電極
２６　回路基板
２８　回路電極
３２　導電性材料
３４　異方性導電接着剤

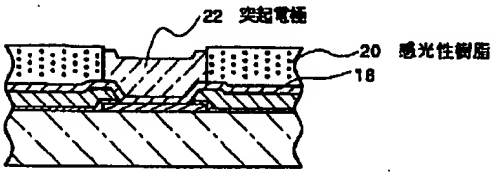
【図１】



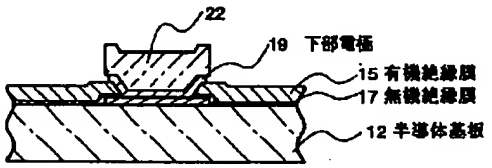
【図２】



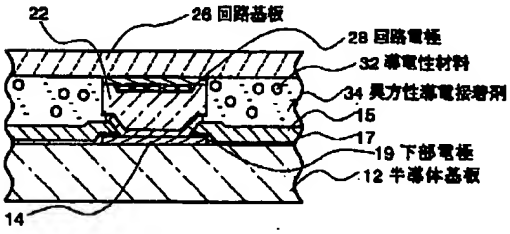
【図３】



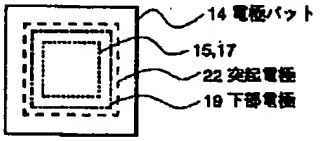
【図４】



【図５】



【図６】



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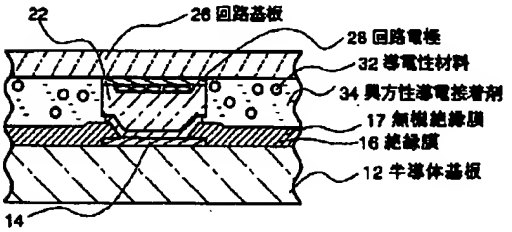

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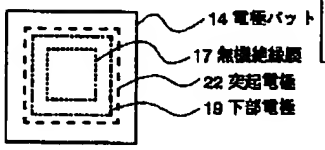
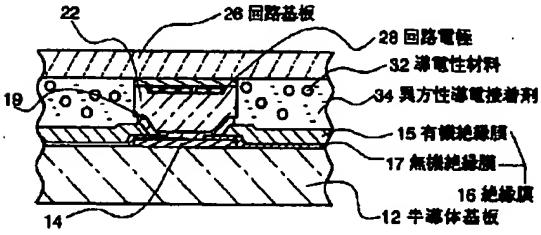
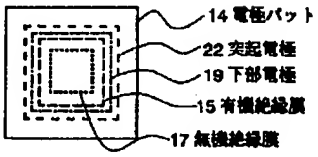


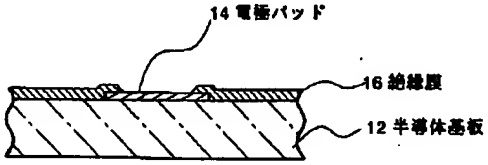
【図９】



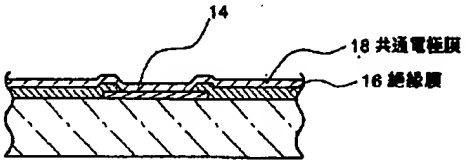
【図１０】



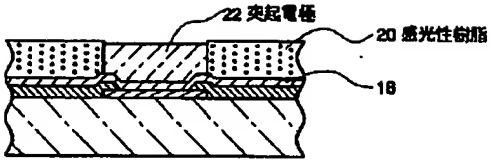
【図１１】



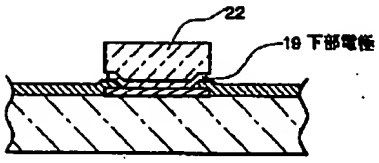
【図１２】



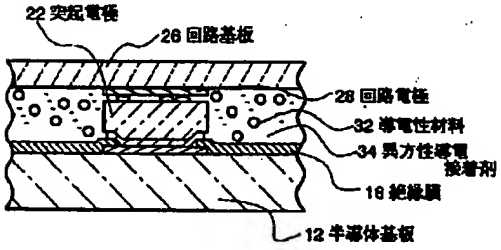
【図１３】


22 突起電極
20 感光性樹脂
18

【図１４】


22
19 下部電極

【図１５】


22 突起電極
26 回路基板
28 回路電極
32 導電性材料
34 異方性導電
接着剤
18 絶縁膜
12 半導体基板